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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:
Deshpande et al.

Serial No.: 10/709,048

Filed: April 8, 2004

Group Art Unit: 2814

Examiner: Ingham, John C.

Atty. Docket No.: FIS920030397US1

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Frederick W. Gibb, III

For: A MANUFACTURABLE METHOD AND STRUCTURE FOR DOUBLE SPACER CMOS WITH OPTIMIZED NFET/PFET PERFORMANCE

Commissioner of Patents
PO BOX 1450
Alexandria, VA 22313-1450

RESPONSE TO RESTRICTION REQUIREMENT

Sir:

In response to the Office Action dated September 30, 2005, please consider the following: